

Application No.: 10/619,483  
Amendment Under 37 C.F.R. §1.111 dated November 1, 2004  
Response to the Office Action of June 2, 2004

### **REMARKS**

This is in response to the Office Action dated June 2, 2004. Claims 1 and 3 – 10 remain pending in the application. Claim 2 was cancelled without prejudice or disclaimer. Claims 3, 9 and 10 were withdrawn from consideration. Claim 7 was merely objected to as depending on a rejected base claim, but is otherwise allowable. The indication of allowable subject matter in claim 7 was much appreciated. The rejections set forth in the Office Action are respectfully traversed below.

### **The Title**

The title was amended above to read “Semiconductor Device with Capacitor.” Accordingly, withdrawal of the objection to the title is respectfully requested.

### **Rejections under 35 U.S.C. §102**

Claims 1 and 2 were rejected under 35 U.S.C. §102 over JP 2001-102512 (JP ‘512). Claims 1, 2, 5, 6 and 8 were rejected under 35 U.S.C. §102 over JP 7-111226 (JP ‘226). However, it is submitted that nothing in the prior art teaches or suggests all the features recited in the present claimed invention.

For instance, amended independent claim 1 recites the capacitor being electrically connected to pads on bottom of the integrated circuit chip, by bonding pads of the capacitor *directly contacting* the pads on the bottom of the integrated circuit chip. There are no intervening elements between the pads of the capacitor and the pads on the bottom of the IC chip

(see e.g., Figs. 3B, 6A, and 6B). Without intervening components between the respective bonding pads, variations in the height of the capacitor when the integrated circuit chip (the semiconductor IC chip 2) with the capacitor (the thin-film capacitor 20) is mounted on the carrier substrate (the package substrate 1) are minimized, which makes it possible to easily control the mounting height (bump height) of the semiconductor IC chip 2 on the package substrate 1.

In contrast, JP '512 requires solder bumps 42 separating the pads on the IC 1 and the pads on the capacitor 5. The intervening solder bumps 42 is contrary to the present claimed limitation for the bonding pads of the capacitor to be *directly contacting* the pads on the bottom of the IC chip. The intervening solder bumps 42 takes away from the ability to compensate for variations in the height of the capacitor when mounting an IC chip having the capacitor to a carrier substrate.

As for JP '226, the capacitor 11 is attached to the bottom surface of the chip 12 with the adhesive 13. The bonding pads of the capacitor 11 are not *directly contacting* the pads on the bottom surface of the chip 12. In addition, solder bumps are used. As with JP '512, there is no teaching in JP '226 for direct contact between bonding pads of the capacitor with pads on the bottom of the IC chip, without intervening solder bumps.

Moreover, amended claim 1 recites the capacitor being provided with a substrate having a bottom surface in contact with a top surface of the carrier substrate on which the integrated circuit chip is mounted (previously recited in claim 2 – now canceled). By having the bottom surface of the substrate of the capacitor being in contact with the top surface of the carrier substrate on which the integrated circuit chip is mounted, it is possible to arrange the bumps

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between the semiconductor IC chip 2 and the package substrate 1 into a cylindrical configuration after the mounting.

JP '226 is further distinguished for the reason that the capacitor substrate is not "in contact with a top surface of the carrier substrate." On the contrary, the capacitor substrate is in contact (through adhesive 13) with the bottom surface of the chip 12.

For at least these reasons, the present claimed invention patentably distinguishes over the prior art.

#### **Rejections under 35 U.S.C. §103**

Claim 4 was rejected under 35 U.S.C. §103 over JP '512 or JP '226, in view of **Chen et al.** (USP 5,548,474). The further reference to **Chen** was made for allegedly disclosing a silicon carrier substrate, as recited in claim 4. However, **Chen** merely describes a *capacitor* substrate that may be made of silicon (column 4, lines 4 – 5), whereas claim 4 is directed to the *carrier* substrate. In addition, claim 4 distinguishes over the prior art for at least the reasons that its base claim 1 distinguishes over the prior art, as explained above. Nothing in the further reference to **Chen** overcomes the deficiencies in the primary references to either JP '512 or JP '226.

For at least the reasons above, the present claimed invention patentably distinguishes over the prior art. Therefore, the present application is in condition for allowance and an early Notice of Allowance is respectfully requested. If for any reason it is believed that this application is not now in condition for allowance, the Examiner is invited to contact applicant's

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undersigned attorney at the telephone number indicated below to arrange for disposition of this case

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully Submitted,

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